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10/022,659	12/18/2001	Kameran Azadet	14-6	1760

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EXAMINER	
TORRES, JUAN A	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 10/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,659	AZADET ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,8-10,12 and 15-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-10,12 and 15-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Regarding claim rejections under 35 U.S.C. 112, second paragraph:

The modifications to the claims were received on 09/14/2006. These modifications are accepted by the Examiner.

In view of the amendment filed on 09/14/2006, the Examiner withdraws claim rejections under 35 USC § 112 second paragraph to claim 12 of the previous Office action.

Regarding claim rejections under 35 U.S.C. 101:

Applicant's arguments filed on 09/14/2006 have been fully considered but they are not persuasive.

The Applicant contends, "Thus, as expressly set forth in claim 16, the claimed method represents an MLT-3 code as a trellis, where the MLT-3 code uses three signal levels (physical things) to represent two binary values. The claimed method generates a trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period. In addition, each of the trellis states has at least two branches leaving or entering each state, with each of the at least two branches corresponding to state transitions associated with the two binary values. A first binary value causes a state transition in the trellis and a second binary value does not cause a state transition in said trellis. This transformation to a trellis representation of an MLT-3 code provides a useful, concrete and tangible result. Applicant submits that claim 16 is

in full compliance with 35 U.S.C. §101, and accordingly, respectfully requests that the rejection under 35 U.S.C. § 101 be withdrawn".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, claim 16 is rejected under 35 USC 101 because the claimed invention as a whole is directed to solely an abstract idea or to manipulation of abstract ideas or does not produce a useful result (emphasis added). Claims 16-22 are directed to a method for representing a trellis, that consists solely of the manipulation of an abstract idea that is not concrete or tangible. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed. Cir.1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459. Claims 16-22 don't produce any practical application that produces a useful, concrete and tangible result State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02 (emphasis added).

For these reasons and the reason stated en the previous Office action, the rejection of claims 16-22 are maintained.

The Examiner wants to direct the attention of the Applicant's representative to the Official Gazette number 1300-4 published November 22, 2005, section "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" attached to this Office action.

Regarding Art rejections claims 16-19 and 22:

Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Regarding Art rejections claims 1 and 8:

Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8, 9, 15 and 27-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 8, 9, 15 and 27-29 are rejected because they are single means claims. A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to Hyatt is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 16-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

As per claim 16, claim 16 is rejected under 35 USC 101 because the claimed invention as a whole is directed to solely an abstract idea or to manipulation of abstract ideas or does not produce a useful result. Claims 16-22 are directed to a method for representing a trellis, that consists solely of the manipulation of an abstract idea that is not concrete or tangible. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed. Cir.1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459. Claims 16-22 don't produce any practical application that produces a useful, concrete and tangible result State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02 (emphasis added).

As per claims 17-22, clams 17-22 are rejected because they depend directly from claim 16, and claim 16 is rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan (US 6418172 B1) in view of Trans (US 6377640 B2).

As per claim 16, Raghavan discloses a method for representing an MLT-3 code as a trellis, the MLT-3 code uses three signal levels to represent two binary values (figure 1A column 3 lines 37-50), the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period (figure 1A column 3 lines 37-50); and generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values (figure 1A column 3 lines 37-50). Raghavan doesn't specifically disclose that a first binary value substantially always maintain causes a state transition in the trellis from a first state to a different state and a secondary binary value does not cause a state transition in the trellis. Trans discloses that a first binary value substantially always maintain causes a state transition in the trellis from a first state to a different state and a secondary binary value does not cause a state transition in the trellis (column 61 lines 48-56). Raghavan and Trans teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the transitions disclosed by Trans. The suggestion/motivation for doing so would have been to reduce the bandwidth of the system (column 61 lines 48-56).

As per claim 17, Raghavan and Trans disclose claim 16. Raghavan also discloses that a first one of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of +1 (figure 1A column 3 lines 37-50).

As per claim 18, Raghavan and Trans disclose claim 16. Raghavan also discloses that a second and third of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of 0 (figure 1A column 3 lines 37-50).

As per claim 19, Raghavan and Trans disclose claim 16. Raghavan also discloses that a fourth one of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of -1 (figure 1A column 3 lines 37-50).

As per claim 22 Raghavan and Trans disclose claim 16. Raghavan also discloses an Ethernet channel (column 1 lines 11-34).

Claims 1, 7, 8, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan (US 6418172 B1) in view of Haratsch ("A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, 21-24 May 2000 Page(s): 465 – 468) (hereafter Haratsch1).

As per claims 1 and 8, Raghavan discloses the MLT-3 encoding (column 1 lines 24-36), Raghavan doesn't disclose decoding a encoded signal received from a dispersive channel causing intersymbol interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis. Haratsch1 discloses decoding a encoded signal received from a dispersive channel causing intersymbol

interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis (title, abstract, introduction, parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan thē joint equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

As per claim 7 and 15, Raghavan and Haratsch1 disclose claims 1 and 8, Raghavan also discloses an Ethernet channel (column 1 lines 11-36).

As per claim 12, Raghavan and Haratsch1 disclose claim 1, Haratsch1 also a branch metric units (BMU) that calculates branch metrics based on said received signal (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4); an add-compare-select unit (ACSU) that determines the best surviving paths into said trellis states (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4); and a survivor memory unit (SMU) that stores said best surviving paths (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of

Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the joint equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Trans as applied to claim 16 above, and further in view of Haratsch ("A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, 21-24 May 2000 Page(s): 465 – 468) (hereafter Haratsch1). Raghavan and Trans disclose claim 16. Raghavan also discloses encoding a signal using MLT-3 code (figure 1A column 3 lines 37-50). Raghavan doesn't disclose using the trellis to perform joint equalization and decoding of an encoded signal. Haratsch1 discloses decoding a encoded signal received from a dispersive channel causing intersymbol interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis (title, abstract, introduction, parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan, Trans and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Trans the joint equalization and decoding disclosed by

Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

Claims 2, 9, 10 and 23-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Haratsch1 as applied to claims 1 and 8 above, and further in view of Haratsch ("High-speed VLSI implementation of reduced complexity sequence estimation algorithms with application to Gigabit Ethernet 1000Base-T", International Symposium on VLSI Technology, Systems, and Applications, 1999. 8-10 June 1999 Page(s): 171 – 174) (hereafter Haratsch2).

As per claims 2 and 9, Raghavan and Haratsch1 disclose claims 1 and 8, Raghavan and Haratsch1 don't disclose a reduced complexity sequence estimation technique. Haratsch2 discloses a reduced complexity sequence estimation technique (title, abstract, introduction, and reduced complexity sequence estimation sections pages 171-174). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claim 10, Raghavan, Haratsch1 and Haratsch2 disclose claim 9, Haratsch2 also discloses a branch metric units (BMU) that calculates branch metrics based on said received signal (reduced complexity sequence estimation section B page

172 figure 4); an add-compare-select unit (ACSU) that determines the best surviving paths into said reduced states (reduced complexity sequence estimation section B page 172 figure 4); a survivor memory unit (SMU) that stores said best surviving paths (reduced complexity sequence estimation section B page 172 figure 4); and a decision-feedback unit (DFU) that takes survivor symbols from said SMU to calculate ISI estimates for said reduced states, wherein said ISI estimates are used by said BMU to calculate branch metrics for transitions in the reduced-state trellis(reduced complexity sequence estimation section B page 172 figure 4). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 23 and 27, Raghavan and Haratsch1 disclose claims 1 and 8. Raghavan and Haratsch1 don't disclose that a state in the trellis is given by a concatenation of the code state and a channel state, where the channel state describes the dispersive channel. Haratsch2 discloses that a state in the trellis is given by a concatenation of the code state and a channel state, where the channel state describes the dispersive channel (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet

communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 24 and 28, Raghavan and Haratsch1 disclose claims 1 and 8. Raghavan and Haratsch1 don't disclose that a state in the trellis is given by a concatenation of the code state and a truncated channel state, where the truncated channel state describes the dispersive channel. Haratsch2 discloses that a state in the trellis is given by a concatenation of the code state and a truncated channel state, where the truncated channel state describes the dispersive channel (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 26 and 29, Raghavan, Haratsch1 and Haratsch2 disclose claims 24 and 28. Haratsch2 also discloses that that number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory (introduction section page 171). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are

from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claim 25, Raghavan, Haratsch1 and Haratsch2 disclose claim 24. Haratsch2 also discloses computing ISI estimates for the states using symbols from corresponding survivor paths (introduction, and reduced complexity sequence estimation sections pages 171-172); computing branch metrics for transitions in the trellis based on the ISI estimates (introduction, and reduced complexity sequence estimation sections pages 171-172); determining survivor paths into the states based on the branch metrics; and storing the survivor paths (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Trans as applied to claim 16 above, and further in view of Haratsch

("High-speed VLSI implementation of reduced complexity sequence estimation algorithms with application to Gigabit Ethernet 1000Base-T", International Symposium on VLSI Technology, Systems, and Applications, 1999. 8-10 June 1999 Page(s): 171 – 174) (hereafter Haratsch2). Raghavan discloses claim 16. Raghavan doesn't disclose combining the trellis with a trellis representing a channel to obtain a super trellis. Haratsch2 also discloses combining the trellis with a trellis representing a channel to obtain a super trellis (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Trans and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the MLT-3 encoding disclosed by Raghavan and Trans the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
9-26-2006